CLAIMS

What is claimed is:

1. A method comprising:

comparing an alignment between an edge of a first clock signal to a center of a data packet to produce an alignment offset signal; and

adjusting the first clock signal using a variable delay device in response to the alignment offset signal to substantially align the edge of the first clock signal to the center of the data packet.

2. The method of claim 1, further comprising:

receiving a second clock signal; and

generating the first clock signal from the second clock signal using the variable delay device.

3. The method of claim 2, wherein variable delay device comprises a delay line.

4. The method of claim 1, further comprising receiving the data packet from a data bus.

5. The method of claim 1, wherein the comparing comprises comparing the first clock signal and the data packet using a quadrature phase detector.

6. An apparatus comprising:

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to align an edge of the first clock signal with a center of a data packet.

7. The apparatus of claim 6, further comprising a clock generator coupled to the first input of the variable delay device to provide a second clock signal to the variable delay device, which generates the first clock signal from the second clock signal.

8. The apparatus of claim 6, wherein the data packet is input to the second input of the detector.

9. The apparatus of claim 6, wherein the variable delay device comprises a delay line.

10. The apparatus of claim 6, wherein the detector comprises a quadrature phase detector.

11. A system comprising:

a plurality of dynamic random access memory (DRAM) devices;

a bus; and

a memory controller comprising:

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to align an edge of the first clock signal with a center of a data packet.

12. The system of claim 11, further comprising a clock generator coupled to the first input of the variable delay device to provide a second clock signal to the variable delay device, which generates the first clock signal from the second clock signal.

13. The system of claim 11, wherein the data packet is input to the second input of the detector from one or more of the plurality of DRAM devices via the bus.

14. The system of claim 11, wherein the variable delay device comprises a delay line.

15. The system of claim 11, wherein the detector comprises a quadrature phase detector.

16. The system of claim 11, further comprising a processor coupled to the memory controller.